Freescale Semiconductor
Technical Data

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Figure 12. Digital Audio Processing Block Diagram

When the DAP block is added in the route, it must be enabled separately to get audio through. It is recommended

```
// SELECT bits 1:0
Modify DAP_SGTL_SURROUND->SELECT 0x0003;
// Ramp down the width to oriaginl value
for (int i = 0; i++; (7 - usOriaginlVal)
{
```

Tabac

5:4	I2S_DOUT	RW	0x1	I

Table 27. CHIP_LINREG_CTRL 0x0026

15	14

The Table 28. CHIP_REF_CTRL 0x0028 register controls the bandgap reference bias voltage and currents.

The Table 29,

Status bits for analog blocks are found in Table 36, CHIP_ANA_STATUS 0x0036

Table 47. DAP_COEF_WR_B0_MSB 0x010E

15	14	13	12	11	10	9	8	7	6	5	4

Table 49. DAP_AUDIO_EQ_BASS_BAND0 0x0116 115 Hz

Table 56. DAP_AVC_CTRL 0x0124

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	RSVD	MAX_GAIN		RSVD		LBI_RESPONSE		RSVD		HARD_LIMIT_EN		RSVD			EN

BITS	FIELD	RW	RESET	DEFINITION
15	RSVD	RO	0x0	Reserved
14	RSVD	RW	0x1	Reserved.
13:12	MAX_GAIN	RW	0x1	Maximum gain that can be applied by the AVC in expander mode. 0x0 = 0 dB gain0x0 0x19 Tc96BT798 0 0 7.98 280.14 536.76 Tm0 Tc0 Tw8x1